UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,903	02/27/2002	Carl Mizuyabu	1376.0200100	4958

34456 7590 05/11/2005

TOLER & LARSON & ABEL L.L.P.
5000 PLAZA ON THE LAKE STE 265
AUSTIN, TX 78746

EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,903	MIZUYABU ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *24-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 36-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to amendment filed on 6 April 2005.

2. Claims 24 – 35 have been cancelled.

3. Claims 44 – 54 have been added new.

4. Claims 1 – 23, and 36 – 54 are pending with the application.

Claim Objections

5. Claims 9, and 15 are objected to because of the following informalities:

6. In the claim 9, too many unnecessary commas creating confusion and complicates the claim language.

7. In the claim 15, too many unnecessary commas creating confusion and complicates the claim language.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1 – 8, 13, 19 – 20, 36 – 38, 44 – 45, 47 – 48, and 52 - 54, are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Mirov et al. [hereinafter as Mirov], US Patent 6,691,2 15 B1.

9. As to claims 1, and 36, Mirov discloses an apparatus and method comprising:

a. determining [based on the bits] a power mode [power mode] for a device [col. 17, 2 8 – 40];

b. disabling [bypassing] a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK UUT] when in a first power mode [idle mode]; and

c. providing the oscillator signal [CLOCK IN] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 - 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines 65 - 67, col. 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64-67, col. 16, lines 1 - 67, col. 17, lines 1 - 54, fig. 5].

10. As to claim 44, Mirov discloses a system comprising:

a. a phase locked loop [PLL] having a first input to receive a first clock signal [CLOCK IN] and a first output to provide a second clock signal [CLOCK OUT], wherein the second clock signal [CLOCK OUT] is based on the first clock signal [CLOCK IN];

b. a first multiplexer [1010] having a first input coupled to thee first input [CLOCK IN] of the phase locked loop [PLL], a second input coupled to the first output of the phase locked loop [CLOCK OUT] and an output, wherein the first multiplexer [1010] is operable to selectively provide [by asserting/deasserting PLL BYPASS signal to selectively output one of the

two inputs] lo the output a signal received at the first input when in a first power mode [idle mode] or a signal received at the second input [second input of 1010 which is output from 1008] when in a second power mode [active mode]; and

c. means [by asserting PLL BYPASS signal] for disabling the phase locked loop when in the first power mode [idle mode][col. 4, lines 43 - 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines 65 - 67, col. 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64- 67, col. 16, lines 1 - 67, col. 17, lines 1 - 54, fig. 5][fig. 10].

11. As to claims 2 – 3, Mirov discloses the computer system different modes [as shown in table 1] including a first mode [idle mode], which consumes less power than in the second power mode [active mode] [col.4, lines 46 – 67, col. 6, lines 57 – 60].

12. As to claims 4 - 5, Mirov discloses clock generator, a phase locked loop circuit, and a bypass circuit for a computer system with an input clock signal [CLK IN] therefore, he teaches different ways of generating clock using crystal oscillator, including RC circuit too [use of crystal oscillator and RC circuit as a different source is inherent to clock generation] [col. 9, lines 26 – 28].

13. As to claims 6, and 7, Mirov discloses coupling of an output of the phase locked loop to a clock divider [1006][col. 12, lines 15 – 35, 54 - 57, fig. 5].

14. As to claim 8, Mirov teaches a power supply comprised of power modules and method of providing reduced power in comparison to available power to the device [col. 21, lines 27 - 67, col. 22, lines 1 - 67, col. 23, lines 1 - 56,fig. 18].

15. As to claim 13, Mirov discloses device including portable electronic device [laptop computers][col. 1, 1ine16 – 17].

16. As to claim 19, Mirov discloses enabling/disabling the phased lock loop including shutting off power used [by removing the VCC input of the AND gate 512 in fig. 7] for driving the phased lock loop [col. 11, lines 10 – 27, col. 21, lines 47 - 67, col. 22, lines 36 – 67, fig. 7].

17. As to claim 20, Mirov discloses providing the oscillator signal [CLOCK IN] to drive a clock line includes coupling [1012, clock tree] a line carrying the oscillator signal [CLOCK IN] to the clock line [CLOCK OUT][co1. 16, lines 16 - 18, fig. 7, and 10].

18. As to claim 37, Mirov discloses the computer system with first mode [idle mode], which consumes less power than in the second power mode [active mode] [col.4, lines 46 – 67, table 1].

19. As to claim 38, Mirov discloses a first number of bits to represent the first power mode and a second number of bits to represent the second power mode [table 1].

20. As to claim 45, Mirov discloses a first clock divider [1006] and coupling of an output of first multiplexer [1010][co1. 12, lines 54 - 57, fig. 5].

21. As to claim 47, Mirov discloses a means [register bits] for determining a power mode [normal, reduced power mode, idle mode, reserved mode, as shown in table 1] of the system and means [asserting/deasserting PLL BYPASS signal] for providing a control signal [PLL BYPASS] to the first multiplexer based on the determined power mode [col. 6, lines 49 – 67, col. 17, lines 26 – 41].

22. As to claim 48, Mirov teaches means for determining a power mode of the system including means [software] for determining a number of pending instructions [maximum utilization and underutilization][col. 4, lines 4, lines 31 – 50, col. 6, lines 49 – 67, col. 7, lines 1 – 24, col. 17, lines 26 – 41].

23. As to claims 52, and 54, Mirov discloses enabling/disabling the phased lock loop including shutting off power used [by removing the VCC input of the AND gate 512 in fig. 7] for driving the phased lock loop [col. 11, lines 10 – 27, col. 21, lines 47 - 67, col. 22, lines 36 – 67, fig. 7].

24. As to claim 53, Mirov discloses an oscillator [506] having and output coupled to the input of the phased lock loop [PLL], and is operable to output the first clock signal [col. 9, lines 15 – 35, fig. 5].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,2 15 B1 as applied to claims 1, and 13 as above.

26. As to claim 14, Mirov discloses an apparatus and method for reducing power consumption of an electronic device such as laptop computers [portable] drawing power from battery [battery operated] [col. 1, lines 17 – 20] but does not

specify what type of electronic devices. The examiner takes Ofticial Notice that laptop and personal digital assistant device [PDA] are well-known types of battery operated portable devices. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention to use a laptop computers or personal digital assistant device for the portable electronic device disclosed by Mirov.

27. Claims 1 – 8, 13, 19 – 20, 36 – 38, 44 – 45, 47 – 48, and 52 – 54, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,2 15 B1, and further in view of Mann et al. [hereinafter as Mann], US Patent 5,877,656. 17.

28. As to claims 1, 36, and 44, Mirov discloses an apparatus and method for reducing power consumption comprising: determining [based on the bits] a power mode [power mode] for a device [col. 17, 28 – 40]; disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK OUT] when in a first power mode [idle mode]; and providing the oscillator signal [CLOCK IN] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 - 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines 65 - 67, col. 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64- 67, col. 16, lines 1 - 67, col. 17, lines 1 - 54, fig. 5].

However, Mirov does not teach arrangement of clock input in detail with commonly used oscillator for clock signal generation and input/output buffer to

provide signal as input to and to drive an output signal from different logical circuit blocks. In summary, Mirov does not teach the use of oscillator and input/output buffer in clock generation and selectively driving the output signal.

Mann discloses an architecture for a programmable clock generator [100, fig. 2] having an input section, clock section, and output section with reference crystal oscillator [142] receives input from reference crystal of input section [101] and output a reference signal through an output line [152] to reference buffer [162], and system clock PLL [144] with PLL output through [154] via multiplexer for selectively driving selected input to output section buffer [104] [col. 4, lines 45 - 67, col. 5, lines 1 - 63, fig. 2].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov and Mann before him at the time of invention was made, to modify the circuit arrangement for receiving input clock signal and driving output signals disclosed by Mirov to include a clock generation with crystal oscillator with use of input/output buffer for driving signals to/from logical blocks, and multiplexer for selectively selecting input signal and driving to an output as taught by Mann in order to obtain PLL-based clock generator which can be electrically configured, erased prior to packaging, reduces cycle time from customer requests to prototypes, and reduces inventory costs and can be field programmed if desired [col. 2, lines 1 - 16, col. 6, lines 60 – 67].

29. As to claims 2 - 3, Mirov teaches that the device [apparatus] with different operating modes with reduced power consumption [co1.4, lines 46 – 67].

30. As to claims 4 - 5, Mirov discloses clock generator, a phase locked loop circuit, and a bypass circuit for a computer system with an input clock signal [CLK IN] therefore he teaches different ways of generating clock using crystal oscillator, including RC circuit too.

31. As to claims 6, and 7, Mirov discloses coupling of an output of the phase locked loop to a clock divider [1006][col. 12, lines 54 - 57, fig. 5].

32. As to claim 8, Mirov teaches a power supply comprised of power modules and method of providing reduced power in comparison to available power to the device [col. 21, lines 27 - 67, col. 22, lines 1 - 67, col. 23, lines 1 - 56,fig. 18].

33. As to claim 13, Mirov discloses device including portable electronic device [laptop computers][col. 1, line16 – 17].

34. As to claim 19, Mirov discloses enabling/disabling the power modules to produce desired voltage and make available the desired current on a line for different operating modes [col. 21, lines 47 - 67, col. 22, lines 36 – 67].

35. As to claim 20, Mirov discloses providing the oscillator signal [CLOCK IN] to drive a clock line includes coupling [1012, clock tree] a line carrying the oscillator signal [CLOCK IN] to the clock line [CLOCK OUT][co1. 16, lines 16 - 18, fig. 10].

36. As to claim 37, Mirov discloses the computer system with first mode [idle mode], which consumes less power than in the second power mode [active mode] [col.4, lines 46 – 67, table 1].

37. As to claim 38, Mirov discloses a first number of bits to represent the first power mode and a second number of bits to represent the second power mode [table 1].

38. As to claim 45, Mirov discloses a first clock divider [1006] and coupling of an output of first multiplexer [1010][co1. 12, lines 54 - 57, fig. 5].

39. As to claim 47, Mirov discloses a means [register bits] for determining a power mode [normal, reduced power mode, idle mode, reserved mode, as shown in table 1] of the system and means [asserting/deasserting PLL BYPASS signal] for providing a control signal [PLL BYPASS] to the first multiplexer based on the determined power mode [col. 6, lines 49 – 67, col. 17, lines 26 – 41].

40. As to claim 48, Mirov teaches means for determining a power mode of the system including means [software] for determining a number of pending instructions [maximum utilization and underutilization][col. 4, lines 4, lines 31 – 50, col. 6, lines 49 – 67, col. 7, lines 1 – 24, col. 17, lines 26 – 41].

41. As to claims 52, and 54, Mirov discloses enabling/disabling the phased lock loop including shutting off power used [by removing the VCC input of the AND gate 512 in fig. 7] for driving the phased lock loop [col. 11, lines 10 – 27, col. 21, lines 47 - 67, col. 22, lines 36 – 67, fig. 7].

42. As to claim 53, Mirov discloses an oscillator [506] having and output coupled to the input of the phased lock loop [PLL], and is operable to output the first clock signal [col. 9, lines 15 – 35, fig. 5].

43. Claims 9 - 12, 15 - 18, 39 – 40, and 46, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent

6,691,215 B 1, and further in view of Mann et al. [hereinafter as Mann], US Patent 5,877,656 as applied to claims 1, and 36, above, and further in view of Zhang et al. (hereinafter as Zhang], US Patent 6,687,322.

44. As to claims 9, and 15, Mirov discloses an apparatus and method for reducing power consumption comprising: determining (based on the bits) a power mode [power mode] for a device [col. 17, 28 – 40]; disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK OUT] when in a first power mode [idle mode]; and providing the oscillator signal [CLOCK IN] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 – 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines 65 - 67, col. 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64-67, col. 16, lines 1 - 67, col. 17, lines 1 - 54, fig. 5].

However, Mirov does not teach arrangement of clock input in detail with commonly used oscillator for clock signal generation and input/output buffer to provide signal as input to and to drive an output signal from different logical circuit blocks. In summary, Mirov does not teach the use of oscillator and input/output buffer in clock generation and selectively driving the output signal.

Mann discloses an architecture for a programmable clock generator [100, fig. 2] having an input section, clock section, and output section with reference crystal oscillator [142] receives input from reference crystal of input section [101] and output a reference signal through an output line [152] to reference buffer

[162], and system clock PLL [144] with PLL output through [154] via multiplexer for selectively driving selected input to output section buffer [104] [col. 4, lines 45 - 67, col. 5, lines 1 - 63, fig. 2].

However, neither Mirov nor Mann teaches a second multiplexor having a first input/output buffer coupled to the input/output buffer of the oscillator, a second input/output buffer coupled to the second input output buffer of the phase locked loop and a third input/output buffer, said multiplexor to: when in a first power mode, pass said source clock signal to said third input/output buffer', and when in a second power mode, pass said locked clock signal to said third input/output buffer; a second clock line coupled to the third input/output buffer of the second multiplexor.

Zhang discloses dual mode clock alignment and distribution with a second multiplexor [510] having a first input/output buffer coupled to the input/output buffer [502] of the oscillator, a second input/output buffer coupled to the second input output buffer of the phase locked loop [PLLOUT] and a third input/output buffer, said multiplexor to: when in a first power mode glow speed), pass said source clock signal to said third input/output buffer [514]; and when in a second power mode [high speed], pass said locked clock signal to said third input/output buffer; a second clock line [CLKO] coupled to the third input/output buffer [514] of the second multiplexor [510] [col. 5, lines 9 - 67, col. 6, lines 1 - 60, fig. 5].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov, Mann, and Zhang before him at the time of invention was made, to modify the circuit arrangement for receiving input clock signal to include

a clock generation with crystal oscillator with use of input/output buffer for driving signals to/from logical blocks, and multiplexer for selectively selecting input signal and driving to an output and driving output signals disclosed by Mirov and Mann to include a second multiplexor as taught by Zhang in order to obtain dual mode clock alignment and distribution devices bypasses the PLL and generates clock with sufficient margins to accommodate the requirements of the PCI mode and support both both lower speed PCI clocking mode and the higher speed PCI-X clocking mode to provide substantial savings in cost while reducing circuit complexity [co. 3, lines 34 – 51].

45. As to claims 10 - 11, 16 - 17, and 39 - 40, Zhang discloses PCI and PCI-X devices therefore he teaches multimedia data including audio, video data [col. 2, 1ines56 - 57, col. lines 4 - 21].

46. As to claims 12, and 18, Zhang discloses providing the oscillator signal (CLKI from 502) to the phase locked loop [504], when in the second power mode [high speed or PCI-X], which includes use of maximum number of bits to represent multimedia data [col. 3, lines 33 - 51, fig. 5].

47. As to claim 46, Zang discloses use of second multiplexer [510] and it's coupling arrangement [fig. 5].

48. Claims 21 - 22, 41, 43, and 48 - 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1 as applied to claims 1, 36, and 44 above, and further in view of Durham et al. [hereinafter as Durham], US Patent 6,785,829 B1.

49. As to claims 21 - 22, 41, 43, and 48 - 50, Mirov discloses an apparatus and method comprising: determining (based on the bits) a power mode [power mode] for a device [col. 17, 28 – 40], disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK OUT] when in a first power mode [idle mode]; and providing the oscillator signal [CLOCK 1N] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 - 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines 65 - 67, col. 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64- 67, col. 16, lines 1 - 67, col. 17, lines 1 - 54, fig. 5].

However, Mirov does not teach steps of identifying a number of pending instructions and types of pending instructions for determining the power mode for a device. In summaryary, he does not teach to determine the time to enter low power mode based on types, and number of pending instructions to be performed.

Durham teaches method and apparatus with low power mode identifying circuit [determining low power mode] including power audit and control circuit for monitoring power dissipation of functional unit within processor. The low power mode circuit [234] examines the low power mode enable signal, the request signal and determine the best time to enter the low power mode depending upon types and number of pending operations or instructions to be performed by the

functional unit [col. 6, lines 41 - 67, col. 7, lines 1 - 16, col. 2, lines 4 - 35, col. 3, lines 26 - 67, col. 4, lines 1 – 24].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov and Durham before him at the time of invention was made, to modify the method and apparatus for reducing power consumption disclosed by Mirov to include a power audit and control circuit for power monitoring including steps of determining types and number of pending instructions to be performed and determine the best time to enter the low power mode as taught by Durham in order to obtain self audit and control of power within functional unit of processor for selectively entering low power mode on per functional unit basis to reduce power dissipation of functional unit [col. 1, lines 57 – 64] and each unit can implement its own power dissipation savings easier and more efficiently than central power dissipation control unit [col. 3, lines 44 – 62].

50. Claims 23, 42, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B 1, and further in view of Mann et al. [hereinafter as Mann]; US Patent 5,877,656 as applied to claims 1, 36, and 44 above, and further in view of Anwyl et al. [hereinafter as Anwyl], US Patent 5,576,738.

51. As to claims 23, 42, and 51, Mirov discloses an apparatus and method for reducing power consumption comprising: determining [based on the bits] a power mode [power mode] for a device [col. 17, 28 – 40]; disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLUCK OUT] when in a first power mode (idle mode); and

providing the oscillator signal [CLOCK IN] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 - 67, col. 5, lines 1 - 8, col. 6, lines 49 - 67, col. 7, lines 1 - 20, col. 8, lines 65 - 67, col. 9, lines 1 - 14, col. 13, lines 14 - 52, col. 15, lines 64- 67, col. 16, lines 1 - 67, col. 17, lines 1 - 54, fig. 5].

However, Mirov does not teach arrangement of clock input in detail with commonly used oscillator for clock signal generation and input/output buffer to provide signal as input to and to drive an output signal from different logical circuit blocks. In summary, Mirov does not teach the use of oscillator and input/output buffer in clock generation and selectively driving the output signal.

Mann discloses an architecture for a programmable clock generator [100, fig. 2] having an input section, clock section, and output section with reference crystal oscillator [142] receives input from reference crystal of input section [101] and output a reference signal through an output line [152] to reference buffer [162], and system clock PLL [144] with PLL output through [154] via multiplexer for selectively driving selected input to output section buffer [104] [col. 4, lines 45 - 67, col. 5, lines 1 - 63, fig. 2].

However, neither Mirov nor Mann, does teach step determining the power mode includes identifying a change in display content. In summary, they do not teach to determine to activate/deactivate the power mode to and from standby mode based on change in display content. Anwyl teaches system with display apparatus with means for detecting changes in image content between

successive frames of input video and method of determining the power mode of display device [by bringing out of low power "standby mode" in response to change in screen content to displayed][col. 4, lines 44 - 67, col. 5, lines 1 – 16].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirror and Mann before him at the time of invention was made, to modify the system for reduced power consumption disclosed by Mirov and Mann to include activation/deactivation of low power mode based on identifying a change in display content [change in screen content between successive frame input video signals] as disclosed by Anwyl in order to obtain a display with power management for controlling display circuitry [col. 4, lines 44 - 67, col. 5, lines 1 – 16].

52. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

53. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Response to Arguments

Re claims 1, and 36, Applicant argues, "Mirov fails to disclose that the PLL BYPASS signal disables a PLL". The examiner disagrees. As admitted by Applicant, "when the PLL BYPASS signal is asserted...the PLL 904 is effectively bypassed". When the PLL 904 is bypassed it is non-operational and therefor disabled (in the broadest reasonable interpretation of the terminology "disabled").

In so much as it is Applicant's position that the limitation "disabling a phased locked loop when in a first power mode" requires disabling clock signals input to the PLL or shutting off power to the PLL", Applicant's contention is not well taken. The claims as written are not so limited. Applicant is reminded that the Examiner will not read limitations into the claims. Moreover, Applicant's own argument in stating what "limitations of disabling a phased lock look *may* include" is evidence that disablement can be achieved in other manners, such as thru bypass.

Re claims 21 and 41, Applicant argues, "Durham fails to disclose or suggest the limitations of wherein determining a power mode includes identifying types of pending instructions as recited". The examiner disagrees and directs Applicant's attention to the last sentences of the paragraph of Durham reproduced in Applicant's arguments on page 13 thereof which state "The low power mode circuit 234 determines the best time to enter the lower power mode based on ongoing internal operations, *pending instructions*, etc. This approach increases unit throughput." and clearly indicate that Durham determines the power mode by considering (i.e. identifying types of) pending instructions.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Nitin C. Patel
April 27, 2005